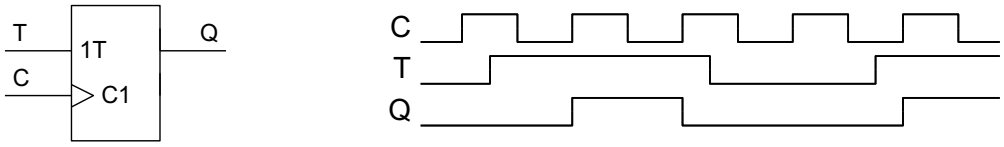
ELEC50001 EE2 Circuits and Systems

Problem Sheet 7 –Timing Constraints & Memory *(Lecture 14 & 15)*

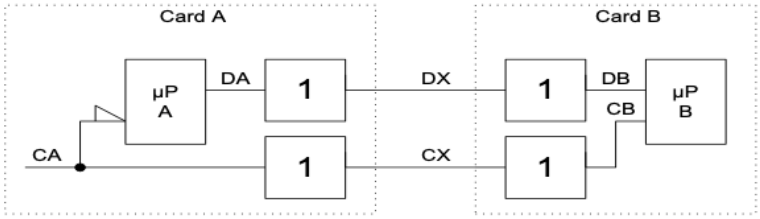
(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. A toggle flipflop (T-flipflop) changes state whenever its T input is high on the CLOCK ↑ edge as shown in the timing diagram.

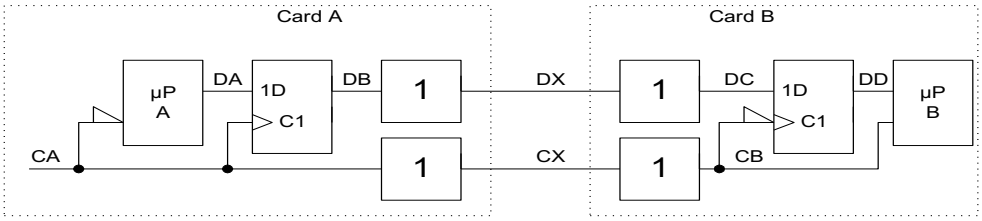


Show how a T-flipflop can be made by combining an XOR gate with a D-flipflop.

2C. A multi-processor system contains two microprocessors which are mounted on separate printed circuit cards. The clock and data signals pass through a line driver when they leave one card and a line receiver when they pass onto the next. The combined delay of the driver+receiver may vary between 13 ns and 22 ns. New data values appear at DA on the falling edge of CA with a propagation delay of 5 to 50 ns. Data is clocked into µP B on the rising edge of CB with a setup time of 12 ns and a hold time of 27 ns. If the clock, CA, is a symmetrical squarewave, calculate its maximum frequency.

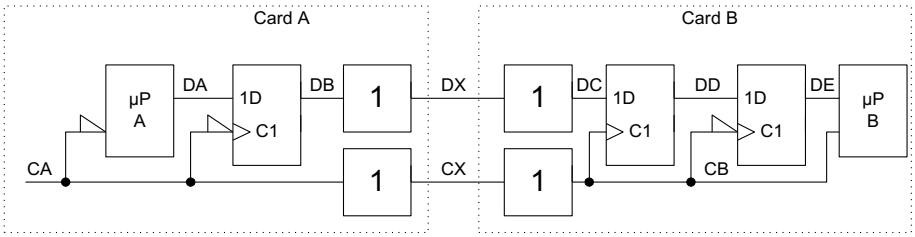


3C. We can speed up the circuit from the previous question by using high-speed flipflops with shorter propagation delays and setup times. The flipflops in the revised circuit have setup and hold times of 5 ns and 3 ns and propagation delays in the range 2 to 10 ns. Note that the second flipflop has an inverted clock. Calculate the new maximum clock frequency by considering its minimum period for each of µPA→flipflop, flipflop→flipflop and flipflop→µPB.



4C. By considering the Hold requirements, explain why the circuit in question 3 would not work if the two flipflops were interchanged.

5D. If we add a third flipflop, we can improve the speed further. Calculate the maximum clock frequency for the following circuit and explain in words how it has achieved the performance increase when compared with the original circuit of question 2.



6A. Explain why most memory integrated circuits have “tri-state” data output pins.

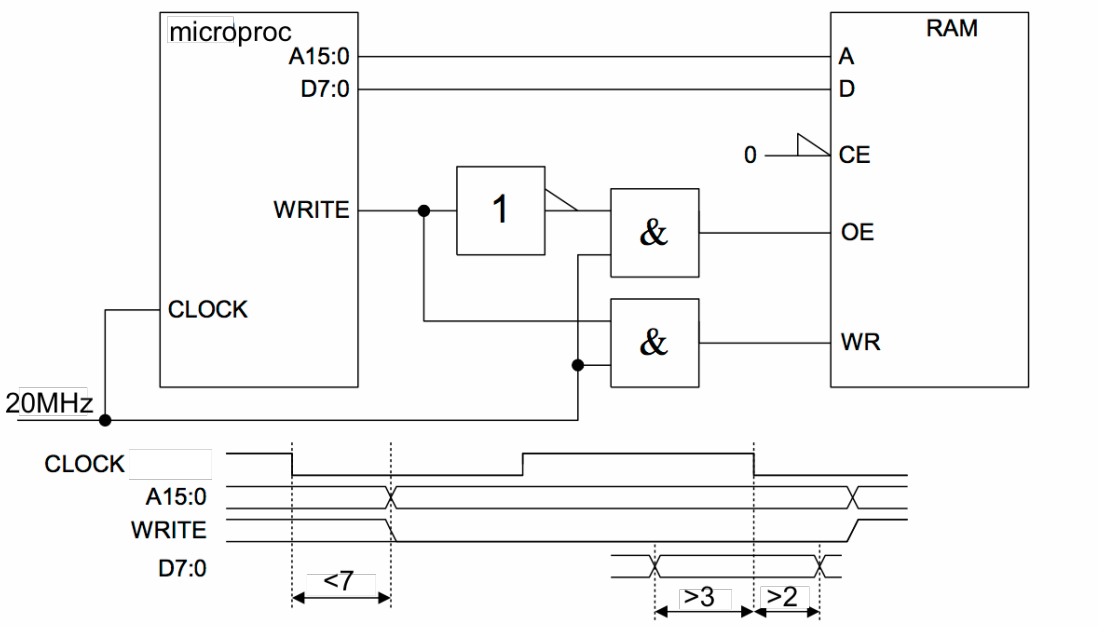
7B. In an 8-bit microprocessor system, addresses 0000 to 9FFF are occupied by RAM and addresses A000 to DFFF are occupied by ROM. The system also contains two peripheral devices: a serial port occupying addresses E100 to E107 and a parallel port occupying addresses E200 to E201. You have a supply of 8k×8 RAM integrated circuits and a supply of 16k×8 ROM integrated circuits.

a) State how many input address pins you would expect to find on each of the RAM integrated circuits, each of the ROM integrated circuits and on each of the peripheral device integrated circuits.

b) Derive Boolean expressions for the CE inputs of each memory and peripheral integrated circuit.

c) Say what is unusual about the byte ordering within the ROM.

8B. The diagram shows an 8-bit microprocessor connected to a memory circuit together with the timing diagram for a microprocessor read cycle..



Each logic gate has a propagation delay that may vary independently in the range 1 to 2 ns. Calculate the maximum permissible access times of the memory from (a) its address inputs, and (b) its OE input.

9A. Explain why a bi-directional buffer is normally designed to have a longer enable time than disable time.